A Denotational Approach to Release/Acquire Concurrency

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Denotational semantics defines the meaning of programs *compositionally*, where the meaning of a program fragment is a function of the meanings assigned to its immediate syntactic constituents. This makes denotational semantics instrumental for understanding the meaning a piece of code in a way that is independent of the context under which the code will run. This style of semantics contrasts with standard operational semantics, which only executes closed/whole programs. A basic requirement of such a denotation function $[\![-]\!]$ is for it to be *adequate* w.r.t. a given operational semantics: plugging program fragments M and N with equal denotations—i.e. $[\![M]\!] = [\![N]\!]$—into some program context $\Xi[-]$ that closes over their variables, results in observationally indistinguishable closed programs in the given operational semantics. Moreover, assuming that denotations have a defined order ($\leq$), a "directed" version of adequacy ensures that $[\![M]\!] \leq [\![N]\!]$ implies that all behaviors exhibited by $\Xi[M]$ under the operational semantics are also exhibited by $\Xi[N]$.

For shared-memory concurrent programming, the seminal work of Brookes [1996] defined a denotational semantics, where the denotation $[\![M]\!]$ is a set of totally ordered traces that consist of sequences of pairs of memory snapshots $\langle \mu_0, \varrho_0 \rangle \dots \langle \mu_n, \varrho_n \rangle$. Each sequence represents a behavior that the program fragment M may exhibit. In every pair $\langle \mu, \varrho \rangle$ in a trace, μ is the snapshot that M relies on the environment to provide; and ϱ is the snapshot that M guarantees to provide in return. The gaps between pairs represent possible interference by the environment. Working under the assumption of preemptive scheduling—imposing no restrictions on the interleaving of steps of execution between parallel threads—denotations are closed under the following two trace-rewriting operations which maintain the representation of possible behavior. *Stutter* adds a transition of the form $\langle \mu, \mu \rangle$ anywhere in the trace; a program fragment can always guarantee no changes between its actions. *Mumble* combines a couple of subsequent transitions of the form $\langle \mu, \varrho \rangle \langle \varrho, \theta \rangle$ into a single transition $\langle \mu, \theta \rangle$ anywhere in the trace; a program fragment can always rely on its own guarantees in the absence of observable interference from the environment.

A *memory model* describes how memory access by concurrently running threads is handled through a program's routine. Brookes established the adequacy of the trace-based denotational semantics w.r.t. the strongest operational semantics of shared-memory concurrent programs, known as *sequential consistency* (SC), where every memory access happens instantaneously and immediately affects all concurrent threads. Jagadeesan et al. [2012] closely followed Brookes to define denotational semantics for x86-TSO [25, 27]. Other weak memory models, in particular, models of *programming languages*, and *non-multi-copy-atomic* models, where writes can be observed by different threads in different orders, have so far been out of reach of Brookes's totally ordered traces, and were only captured by much more sophisticated models based on *partial orders* [10, 12, 16, 18, 20, 26]. Progressing in this direction, we target the Release/Acquire (RA) memory model. This model, obtained by restricting the C/C++11 memory model [2] to release/acquire atomics, is a well-studied fundamental memory model weaker than x86-TSO, which, roughly speaking, ensures "causal consistency" together with "per-location-SC" and "RMW (read-modify-

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write) atomicity" [21, 22]. These guarantees make RA sufficiently strong for implementing common synchronization idioms.

Our first contribution is a Brookes-style denotational semantics for RA. As Brookes's traces are totally ordered, this result may seem counterintuitive. The standard semantics for RA is a declarative (a.k.a. axiomatic) memory model, in the form of acyclicity consistency constraints over partially ordered candidate execution graphs. Since these graphs are not totally ordered, one might expect that Brookes's traces are insufficient. Nevertheless, we observe that Kang et al.'s "view-based" machine [2017], an interleaving *operational* semantics that is equivalent to RA's declarative formulation lends itself to Brookes-style semantics by developing a compatible notion of traces.

In RA's operational semantics, the memory associates a timeline to each location. A thread writes by sending an immutable message, placing it on the appropriate timeline. The message occupies a segment of the timeline that must not intersect already-occupied segments, which means that timeline totally orders the messages. A thread can spontaneously receive a message from memory if a certain to-be-described causal consistency condition is met. Execution starts with a single initial message on each timeline, which threads consider as already received.

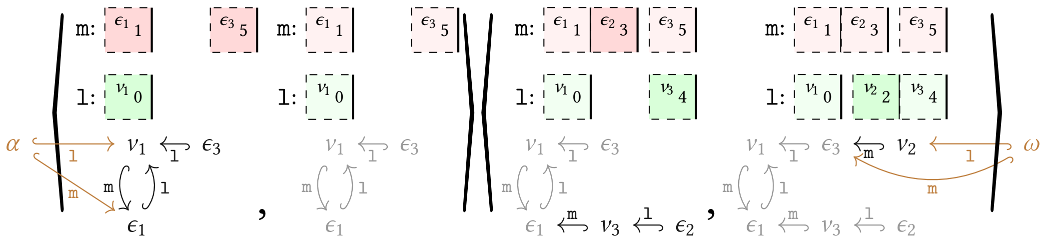
Each thread maintains a view that points to its most recent message at each location: the one that appears latest on the location's timeline of all the messages that the thread has received. A thread reads by loading the value from its most recent message. When a thread writes, it must place the message somewhere after its most recent message on the timeline, though possibly before messages it has not yet received. A message from an RMW's write must be placed adjacently to the read message. This blocks another RMW from doing the same, thus enforcing atomicity. A sent message is considered to be received, and thus it become the thread's most recent message.

Each message records the view of the thread that wrote it, except for initial messages who's view points to the initial messages. We think of messages as pointing to other messages according to this view. A thread can receive any message so long as it has already received all the other messages to which the message points. This mechanism maintains causal consistency: a thread cannot receive a message without receiving the messages that contributed to its creation.

In Kang et al.'s language, as is common in the literature on memory models, parallel composition ($\parallel$) appears only at the top level. We extend this language by allowing ($\parallel$) to appear in nested positions, making it a first-class program construct. This allows us to decompose the justification of Write-Read Reordering (WR-Reord) $(\mathtt{l} := v)\,;\mathtt{m}? \twoheadrightarrow \mathbf{let}\,\mathtt{x} = \mathtt{m}?\,\mathbf{in}\ (\mathtt{l} := v)\,;\mathtt{x}$, a crucial reordering of memory accesses validated by RA but not by SC, using several valid transformations that are justified by independent arguments. The main ones are Write-Read Deorder (WR-Deord) $\langle(\mathtt{l} := v), \mathtt{m}?\rangle \twoheadrightarrow (\mathtt{l} := v) \parallel \mathtt{m}?$ and sequencing $M \parallel N \twoheadrightarrow \langle M, N\rangle$. The latter is an example of a law of parallel programming [14]. With first-class parallelism we can validate the rest too, such as generalized sequencing $(M_1\,;M_2) \parallel (N_1\,;N_2) \twoheadrightarrow (M_1 \parallel N_1)\,;(M_2 \parallel N_2)$. These transformations can occur anywhere in the program, so reasoning in this way requires allowing nested parallelism.

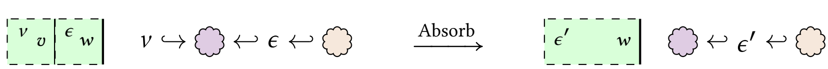
We support first-class parallelism by organizing thread views in an evolving "view-tree", rather than in a fixed flat mapping. When sub-threads are activated, they inherit the view of the parent thread, replacing the corresponding leaf with a node with two child leaves carrying the same view; and when the threads synchronize, the parent thread inherits their views, combining two sibling leaves into a leaf that replaces their parent.

Below we illustrate an example trace, in the setting of two memory locations `l` and `m`. The memory snapshots are illustrated using two diagrams. Top: shows the messages per location as (possibly adjacent) segments on the location's timeline. Bottom: shows the graph structure induced by the views within messages. The only *local* message—added within a transition—is v_2: one that the program fragment guarantees to provide, rather than relies on receiving. Our traces also include an initial view α, and a final view ω, by which the program fragment respectively relies on, and guarantees, availability of message. These views are illustrated by showing where they point.



We prove several results about our semantics. **Soundness:** for every interrupted execution there is a corresponding single-transition trace in the denotation. **Fundamental Lemma:** for every trace in the denotation there exists an interrupted execution of the program fragment exhibiting a related behavior. **Adequacy:** denotational approximation implies contextual refinement. An immediate practical application of adequacy is the ability to provide *local* formal justifications of program transformations, such as performed by optimizing compilers. Formally justifying these transformations without the local analysis that denotational semantics provides is non-trivial [12, 28].

An important aspect of denotational semantics is its abstraction. As an external measure, we verify that our adequate semantics validates various transformations/optimizations: standard and structural transformations; algebraic laws of parallel programming; and all known thread-local RA-valid compiler transformations involving atomic RA memory accesses. This level of abstraction is achieved thanks to our denotations being closed not only under analogs to Brookes's stutter and mumble, but also several RA-specific operations. This design allows us to relate programs which would naively correspond to rather different sets of traces. For example, we have the *Absorb* closure rule, which combines two adjacent local messages added within the same transition. Below we sketch how it modifies memory snapshots between the precedent and antecedent traces:



Figuratively, the preceding message (ν) is "absorbed" by the successor (ϵ which becomes ϵ'). Nothing must point to the preceding message, so as to not leave dangling names. We use this rule when validating transformations which eliminate a write that is followed by another, such as Write-Write Elimination (WW-Elim) $\texttt{l} := v\,; \texttt{l} := w \twoheadrightarrow \texttt{l} := w$.

Our second contribution is to connect the core semantics of parallel programming languages exhibiting weak behaviors to the more standard semantic account for sequential programming languages. Brookes presented his semantics for a simple imperative WHILE language, but Benton et al. [2016], Dvir et al. [2022] later extended it to higher-order languages using Moggi's monad-based approach [1991]. A denotational semantics given in this monadic style comes ready-made with a rich semantic toolkit for program denotation [5], transformations [3, 6–8, 15], reasoning [1, 23], etc. We want to challenge, compare, and reuse this diverse toolkit in the concurrent setting. As a yardstick to the applicability of the monadic toolkit, we develop our semantics for a *higher-order functional language* with a general, first-class parallel composition operator. This is in contrast to most of the weak memory models research which employs imperative languages and assumes a single top-level parallel composition, but more in line with game models for concurrency [e.g. 11]. This puts weak memory models, which often require bespoke and highly specialized presentations, on a similar footing to many other programming effects.

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APPENDIX

The table below summarizes the transformations that we have validated using our denotational semantics. Some are given first using the general **rmw** construct, then specialized to loads (?) and well-known RMWs (CAS, FAA, XCHG). When a non-trivial closure rule (Ab, Ti, Di) is used for the denotational justification it appears above the symbol $\twoheadrightarrow$.

Generalized Sequencing

$(\textbf{let}\,x = M_1\,\textbf{in}\,M_2) \parallel (\textbf{let}\,y = N_1\,\textbf{in}\,N_2) \twoheadrightarrow \textbf{match}\,M_1 \parallel N_1\ \textbf{with}\,\langle x, y\rangle.\, M_2 \parallel N_2$

Sequencing $M \parallel N \twoheadrightarrow \langle M, N\rangle$

Irrelevant Read Introduction $\langle\rangle \twoheadrightarrow \ell?\,;\langle\rangle$

Irrelevant Read Elimination $\ell?\,;\langle\rangle \twoheadrightarrow \langle\rangle$

Write-Write Elimination

$\ell := w\,;\ell := v \overset{\text{Ab}}{\twoheadrightarrow} \ell := v$

Write-Read Deorder $(\ell \neq \ell')$

$\langle \ell := v, \ell'?\rangle \overset{\text{Ti}}{\twoheadrightarrow} \ell := v \parallel \ell'?$

RMW Expansion $(\varphi_{\vec{v}} \leq \psi_{\vec{w}})$

$\textbf{rmw}_{\varphi}\,(\ell;\vec{v}) \overset{\text{Di}}{\twoheadrightarrow} \textbf{rmw}_{\psi}\,(\ell;\vec{w})$

$\ell? \overset{\text{Di}}{\twoheadrightarrow} \text{CAS}\,(\ell, v, v)$

$\text{CAS}\,(\ell, v, v) \overset{\text{Di}}{\twoheadrightarrow} \text{FAA}\,(\ell, 0)$

Atomic Store

$\ell := v \twoheadrightarrow \text{XCHG}\,(\ell, v)\,;\langle\rangle$

Symmetric-Monoidal Laws, e.g.

$M \parallel N \twoheadrightarrow \textbf{match}\,N \parallel M\ \textbf{with}\,\langle x, y\rangle.\,\langle y, x\rangle$

Write-RMW Elimination

$\ell := v\,;\textbf{rmw}_{\varphi}\,(\ell;\vec{w}) \overset{\text{Ab}}{\twoheadrightarrow} \ell := \varphi^{\text{id}}_{\vec{w}} v\,;v$

$\ell := v\,;\ell? \twoheadrightarrow \ell := v\,;v$

$\ell := v\,;\text{CAS}\,(\ell, v, u) \overset{\text{Ab}}{\twoheadrightarrow} \ell := u\,;v$

$\ell := v\,;\text{CAS}\,(\ell, w, u) \twoheadrightarrow \ell := v\,;v \quad (v \neq w)$

$\ell := v\,;\text{FAA}\,(\ell, w) \overset{\text{Ab}}{\twoheadrightarrow} \ell := v + w\,;v$

$\ell := v\,;\text{XCHG}\,(\ell, w) \overset{\text{Ab}}{\twoheadrightarrow} \ell := w\,;v$

RMW-Write Elimination $(\text{dom}\,\psi_{\vec{w}} \supseteq \text{dom}\,\varphi_{\vec{u}})$

$\textbf{let}\,x = \textbf{rmw}_{\varphi}\,(\ell;\vec{u})\ \textbf{in}\ \textbf{match}\,(\psi_{\vec{w}})\,x\,\textbf{with}\,\{\iota_{\bot}\,\_.x \mid \iota_{\top}\,v.\ell := v\,;x\} \overset{\text{Ab}}{\twoheadrightarrow} \textbf{rmw}_{\psi}\,(\ell;\vec{w})$

$\textbf{let}\,x = \ell?\,\textbf{in}\,(\textbf{if}\,x = v\ \textbf{then}\,\ell := w\,\textbf{else}\,\langle\rangle)\,;x \twoheadrightarrow \text{CAS}\,(\ell, v, w)$

$\textbf{let}\,x = \ell?\,\textbf{in}\,\ell := x + v\,;x \twoheadrightarrow \text{FAA}\,(\ell, v)$

$\textbf{let}\,x = \ell?\,\textbf{in}\,\ell := v\,;x \twoheadrightarrow \text{XCHG}\,(\ell, v)$

RMW-RMW Elimination $\langle \textbf{rmw}_{\varphi}\,(\ell;\vec{v}), \textbf{rmw}_{\psi}\,(\ell;\vec{w})\rangle \overset{\text{Ab}}{\twoheadrightarrow} \textbf{let}\,x = \textbf{rmw}_{\zeta}\,(\ell;\vec{u})\ \textbf{in}\ \langle x, \varphi^{\text{id}}_{\vec{v}} x\rangle \quad (\zeta_{\vec{u}} = \psi_{\vec{w}} \circ^{\text{id}} \varphi_{\vec{v}})$

$\langle \ell?, \ell?\rangle \twoheadrightarrow \textbf{let}\,x = \ell?\,\textbf{in}\,\langle x, x\rangle \qquad \langle \text{FAA}\,(\ell, v), \text{FAA}\,(\ell, w)\rangle \twoheadrightarrow \textbf{let}\,x = \text{FAA}\,(\ell, v + w)\ \textbf{in}\ \langle x, x + v\rangle$

$\langle \ell?, \text{CAS}\,(\ell, v, w)\rangle \twoheadrightarrow \textbf{let}\,x = \text{CAS}\,(\ell, v, w)\ \textbf{in}\ \langle x, x\rangle \qquad \langle \text{XCHG}\,(\ell, w), \ell?\rangle \twoheadrightarrow \textbf{let}\,x = \text{XCHG}\,(\ell, w)\ \textbf{in}\ \langle x, w\rangle$